CLAIMS

What is claimed is:

1. A method of single-step interruption debugging applied in a peripheral component interconnect (PCI) bus cycle, which comprises the steps of:

sending out a request signal (REQ#) from a bus master to request for the control of the bus cycle;

locking the signal states such as the address, data, command and byte enable (BE#) of the bus cycle and displaying them through a display;

sending out the address, the command, a frame signal (FRAME#) and an IRDY# ready signal in the next bus cycle after a PCI arbiter responds a acknowledge signal (ACK#);

decoding the address and command through a target device and sending out a device selection signal (DEVSEL#) from the target device;

displaying the signal states such as the address, the data, the command, the byte enable locked in the previous bus cycle on the display; and

sending out a TRDY# ready signal through a switch to end the PCI bus cycle.

2. The method of claim 1, wherein the step of sending out a device selection signal from the target device is achieved by maintaining the device selection signal at LOW so as to suspend the actions on the PCI bus during the bus master cycle.

3. The method of claim 1, wherein the step of ending the PCI bus cycle is achieved by raising the device selection signal to HIGH at the same time the IRDY# ready signal finishes so as to notify the bus master to end the bus cycle.

4. The method of claim 1, wherein the switch comprises a de-bounce circuit to eliminate unexpected de-bouncing generated during the on/off switch.

5. A single-step interruption debug card applied to a peripheral component interconnect (PCI) bus cycle, which debug card comprises:

an address/command lock control logic circuit for generating an address/command control signal and locking the address/command through an address/command locker;

an address/command buffer control logic circuit, which outputs a control signal through the locked address/command to an address/command buffer;

a data/byte enable (BE#) signal lock control logic circuit for generating the lock control signal of a data/BE# bus and locking the data/BE# signal using a data/BE# signal locker;

a bus master control signal generating logic circuit for sending out a request signal (REQ#) to request for the control over the bus; and

a switch, which sends out a TRDY# ready signal to notify the bus master on the PCI bus cycle single-step interruption debug card to end the PCI bus cycle.

6. The debug card of claim 5, wherein the address/command lock control logic circuit further comprises an address/command decoding logic circuit for decoding the address/command so as to determine whether the address/command is a target device in the PCI bus cycle.

7. The debug card of claim 6 further comprising that a device selection signal (DEVSEL#) is sent out in the next PCI bus cycle as a response using a device selection signal generating logic circuit when the target device is in the PCI bus cycle.

8. The debug card of claim 5, wherein the address/command buffer displays through a

display circuit the address/command to perform inspection.

9. The debug card of claim 5, wherein the data/BE# signal locker displays through a display circuit the data/BE# to perform inspection.

10. The debug card of claim 5, wherein the bus master control signal generating logic circuit displays the address/data signal states locked in the previous PCI bus cycle on a display through a bus master address/data generating logic circuit.

11. The debug card of claim 5, wherein the bus master control signal generating logic circuit displays the command/BE# signal states locked in the previous PCI bus cycle on a display through a bus master command/BE# generating logic circuit.

12. The debug card of claim 5, wherein the PCI bus cycle is ended by raising the device selection signal to HIGH when the TRDY# ready signal finishes so as to notify the bus master on the PCI bus cycle single-step interruption debug card to end the PCI bus cycle.

13. The debug card of claim 5, wherein the switch utilizes a de-bounce circuit to eliminate unexpected de-bouncing during the on/off switch.